FPGA and ASIC Forth Market

SVFIG Forth day

November 16, 2024

Christopher Lozinski
EE M.Sc. 9/24

lozinski@PythonLinks.info

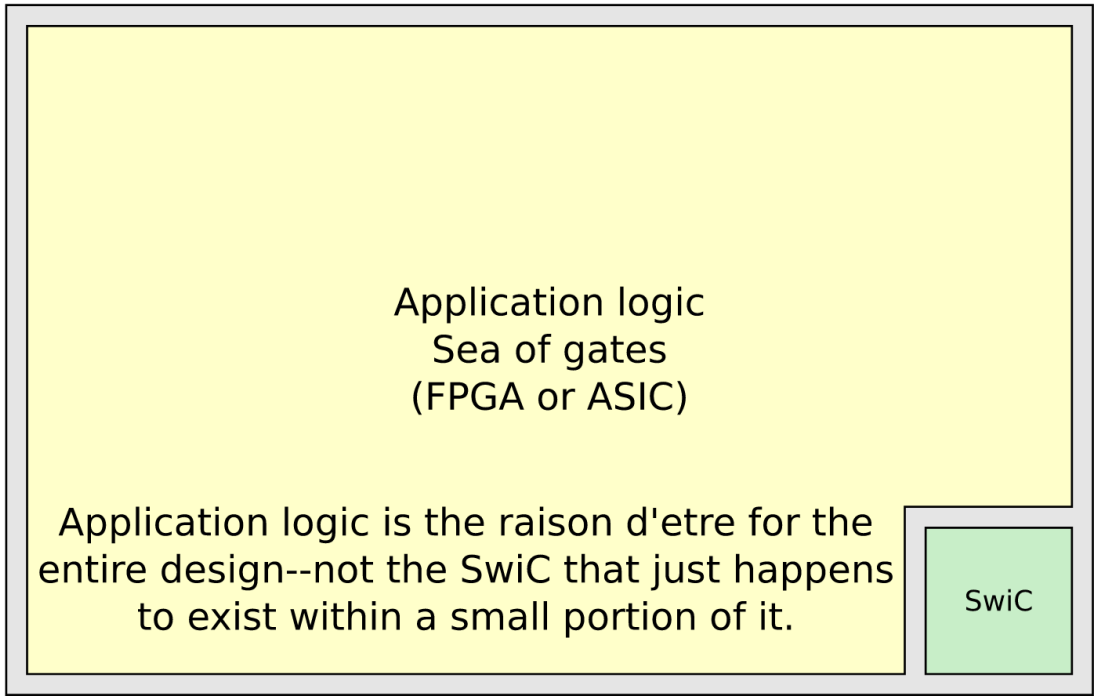
@PythonLinks@Mastodon.Social

Forth Discord Server

Pico-Ice Discord Server

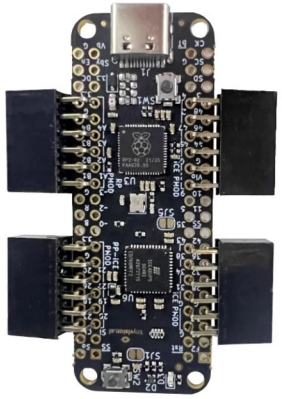
Hana-1 Discord Channel

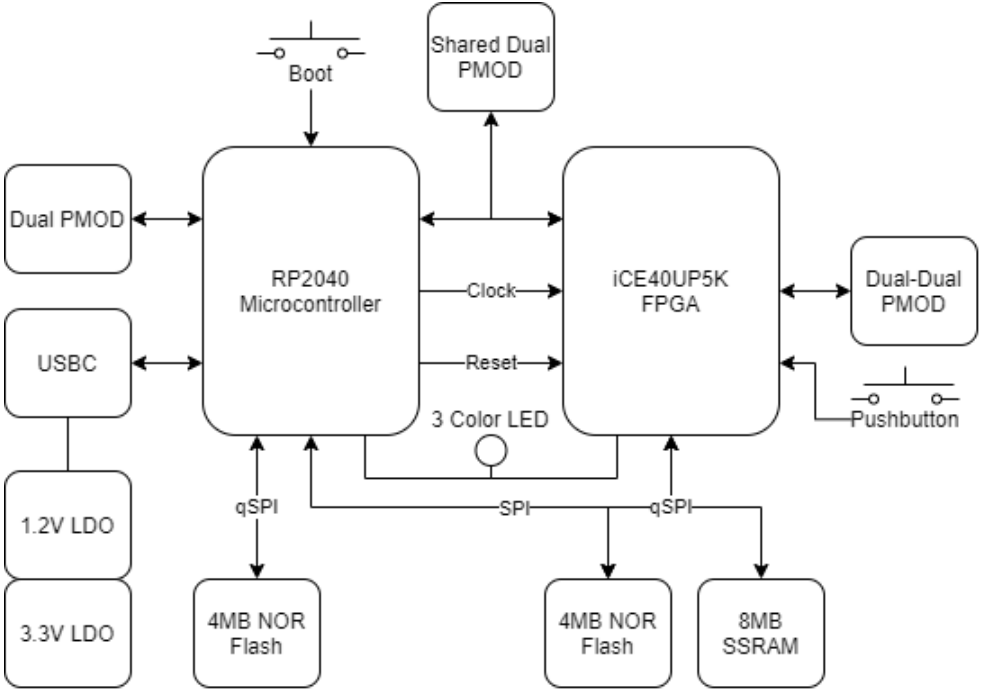
Forth Soft Core on FPGA



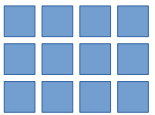
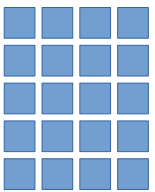
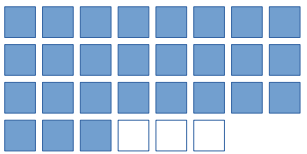
When the finite state machine gets too complex, engineers move to a soft core cpu. Usually RISC-V, but not Forth.

Open Source Pico-Ice Hardware





My Thesis

OLD ICE40LP-1k	NEW ICE40UP5K
 3K App Words  5K System Words Pseudo dual port 32 * 4kbits = 128Kbits PSRAM 8k * 16 bit words.	 30 * 4kbits = 120Kbits of PSRAM 10**14 words Single Port 10**14 words Single Port 10**14b words Single Port 10**14 words Single Port 4* 16Kbits = 1MBit SPRAM

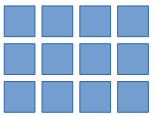
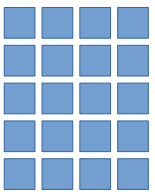
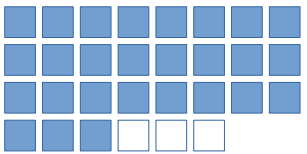
Required Resources

	Stack Depth	LUTs	SPRAMs	BRAMS	Max Frequency (Mhz)	Total Memory (Words)
J1a	15/17	1162		30	?	8192
Mecrisp Ice J1a	32	2141		30	19.45	7680
Hana 1 on BRAMs	256	1183		30	21.60	7168
Hana 1 on SPRAM	256	1043	1-3	3	25.18	16K - 42K

J1 Vs Mecrisp Vs Hana 1

	J1	Mecrisp Ice 16bit PSRAM	Hana 1 16 bit SPRAM
LUTs	1162	2141	1043
Instructions	16	22	26
Shifters	2	5	6
Stack Depth	15/17	32	512
Data Bus		Yes	Yes
SPI		Bit Banged	Shift Register
Timer		Yes	Yes
Max Frequency		17.45 Mhz	23.12 MHz

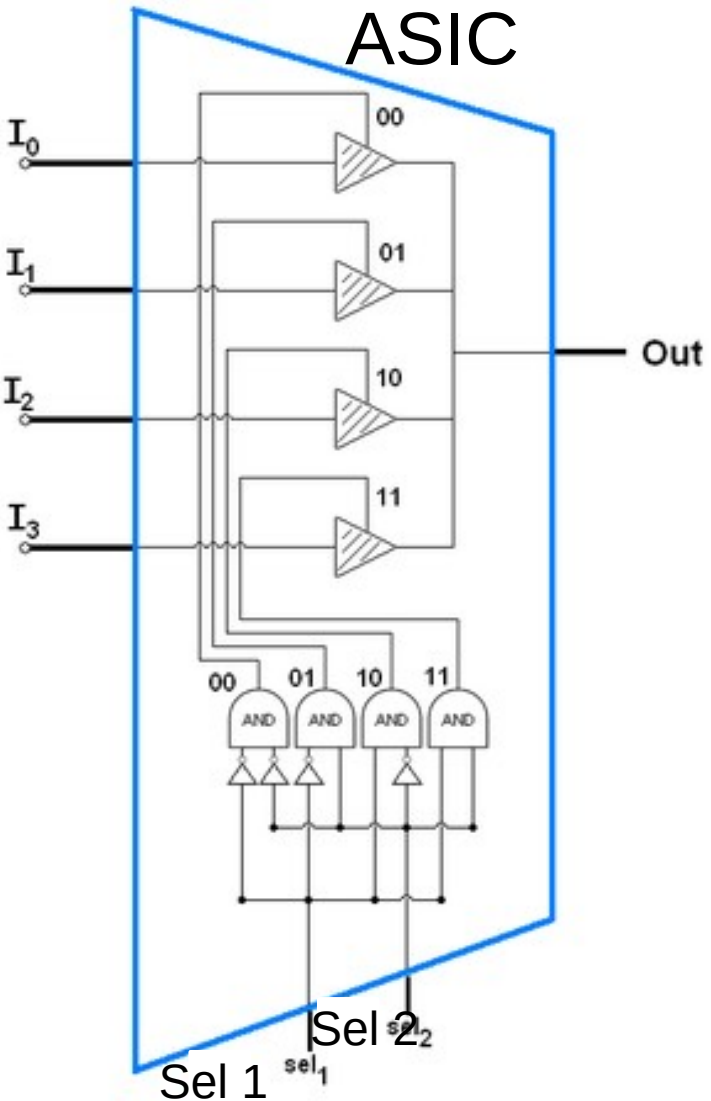
How is That Possible?

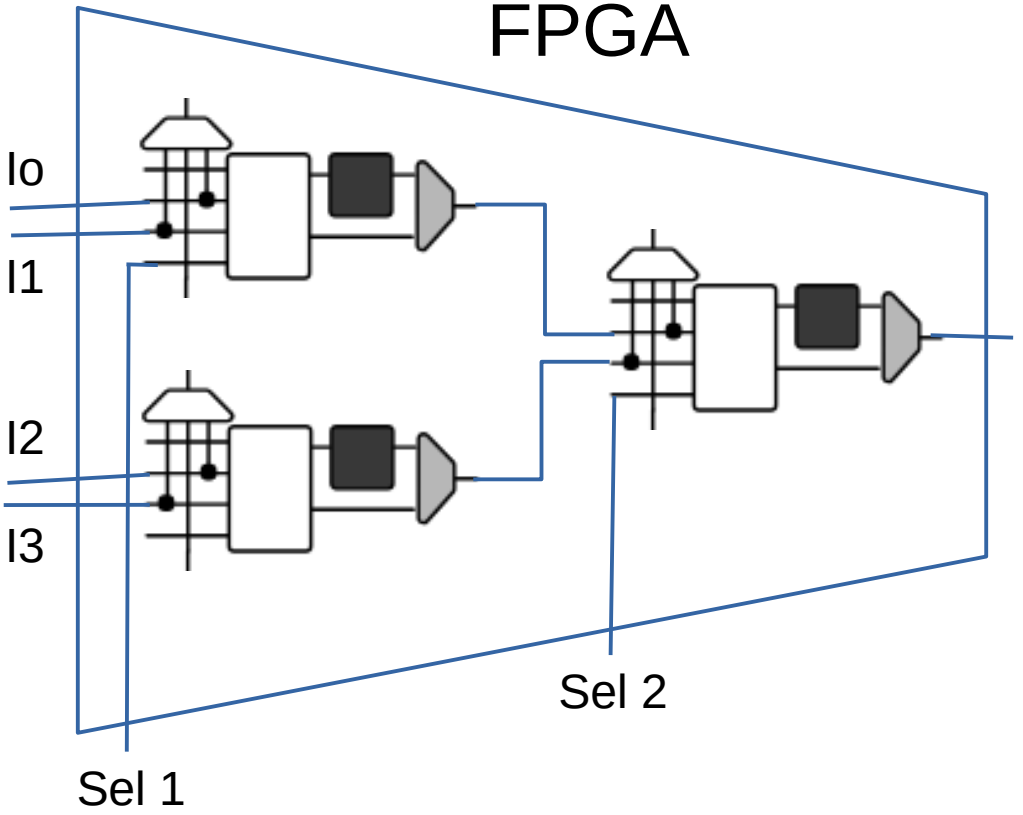
OLD ICE40LP-1k	NEW ICE40UP5K
 3K App Words  5K System Words Pseudo dual port 32 * 4kbits = 128Kbits PSRAM 8k * 16 bit words.	 30 * 4kbits = 120Kbits of PSRAM 10**14 words Single Port 10**14 words Single Port 10**14b words Single Port 10**14 words Single Port 4* 16Kbits = 1MBit SPRAM

Hana 1, ½ the RISC-V Size

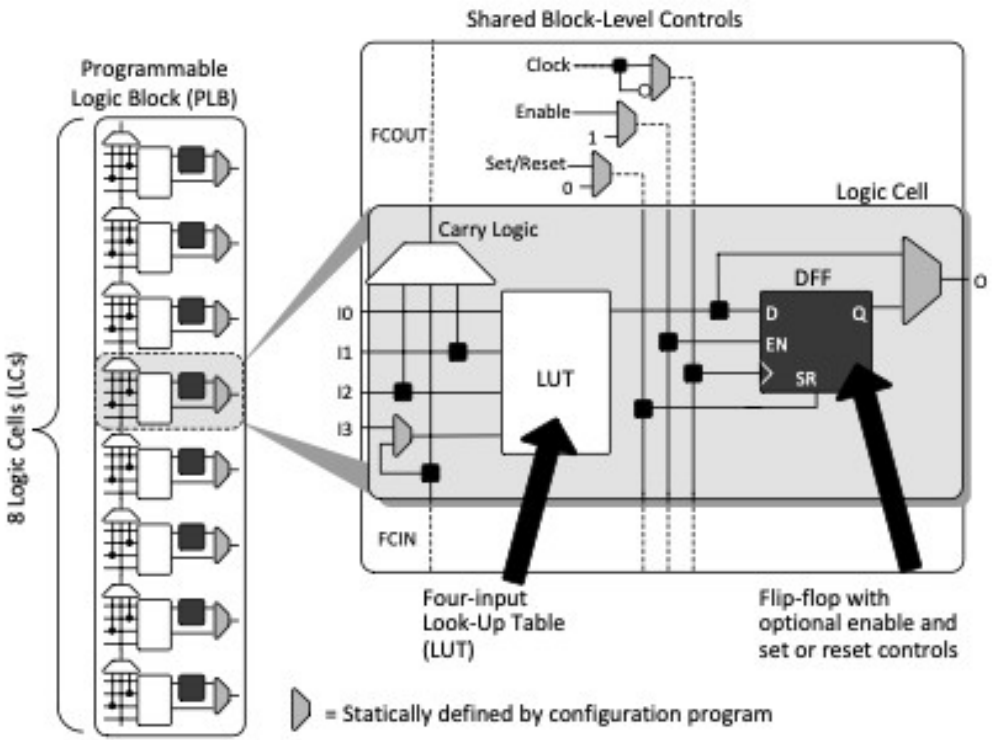
	1162 LUTs	SwapForth J1a
-	140 LUTs	Remove the Memory Multiplexer
-	512 LUTs	Use BRAMs for two 16 deep 16 bit stacks
	500 LUTs	The size of the Bit Serial RISC-V Serve CPU.
	1150 LUTs	Typical small RISC-V size.

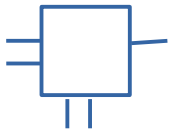
Multiplexers



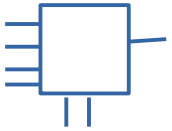


Programmable Logic Block

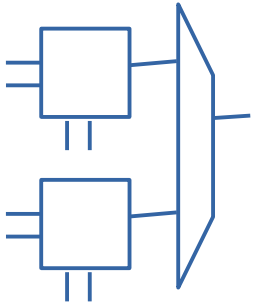




Ice40 4 input Luts

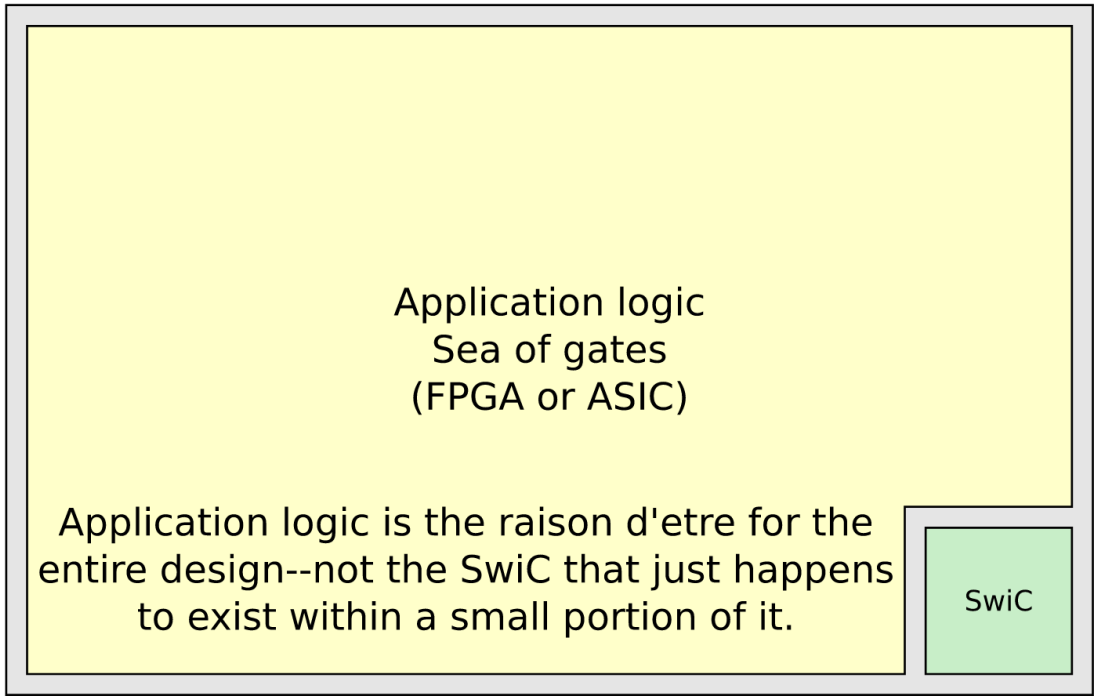


Xilinx 6 input Luts



Cologne Chip
Lut tree

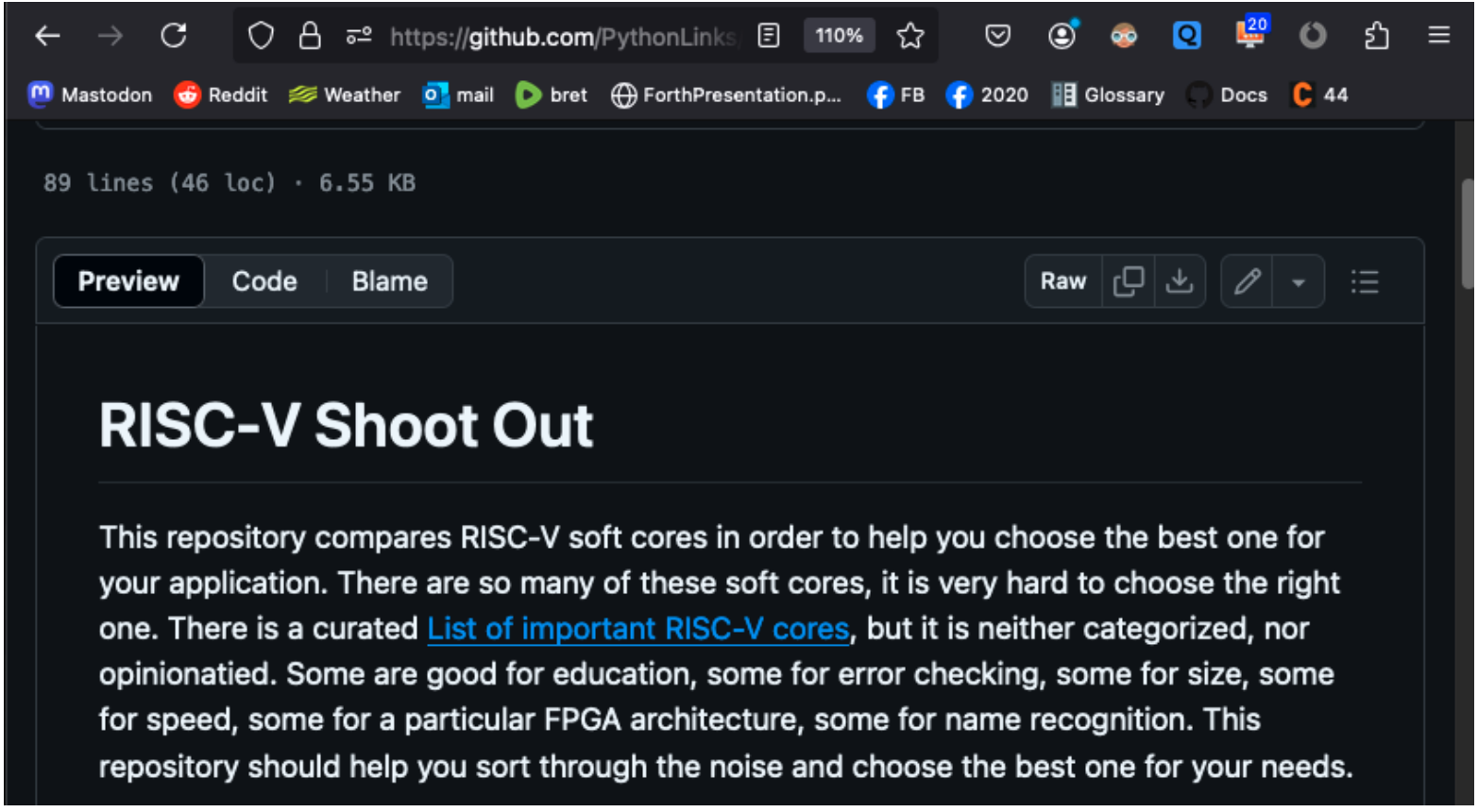
Everyone Wants RISC-V on FPGA



When the finite state machine gets too complex, engineers move to a soft core cpu. Usually RISC-V, but not Forth.

Lots of RISC-V Soft Cores

https://github.com/PythonLinks/risc-v-shoot-out



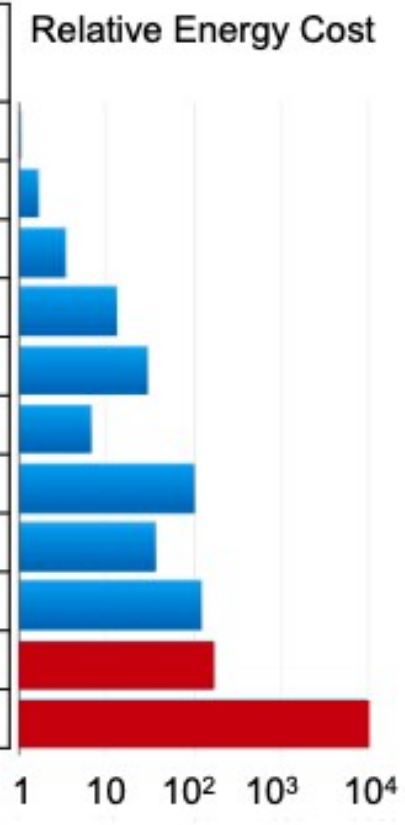
RISC-V Python Vs Forth Memory Requirements

MicroPythons minimum requiremenst are 256KByte of ROM and 16KB RAM.	Mecrisp nucleus requires 6.5KBytes + Application space No ROM. On ICE40.
Snek requires 32KBytes ROM + 2 K Byte RAM	11 kBytes of flash and 512 bytes of RAM on MSP430
The Lua interpreter takes 282KBytes and the Lua library takes 470KBytes.	
eLua requires 256KBytes of ROM, + 32 KBytes of RAM.	

ROM is slower than RAM

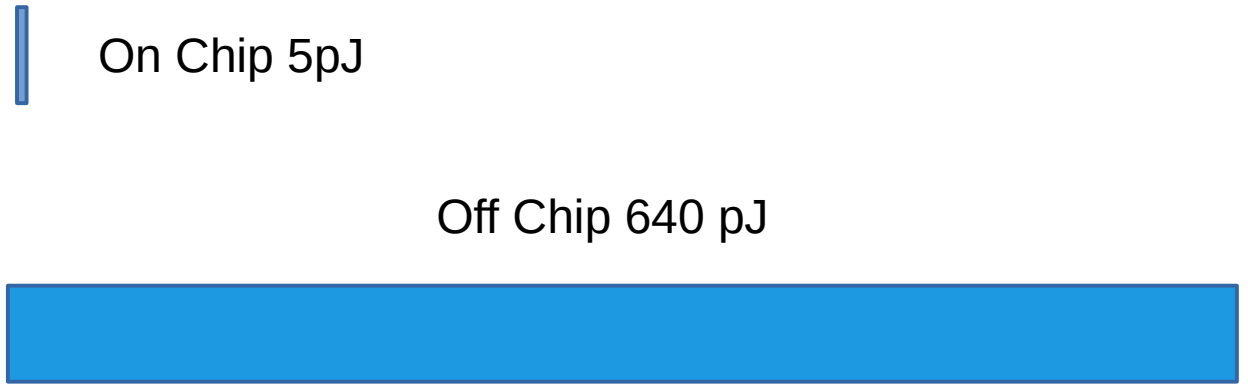
POWER

Operation:	Energy (pJ)
8b Add	0.03
16b Add	0.05
32b Add	0.1
16b FP Add	0.4
32b FP Add	0.9
8b Mult	0.2
32b Mult	3.1
16b FP Mult	1.1
32b FP Mult	3.7
32b SRAM Read (8KB)	5
32b DRAM Read	640



Memory access is **orders of magnitude** higher energy than compute

Power For Memory Access



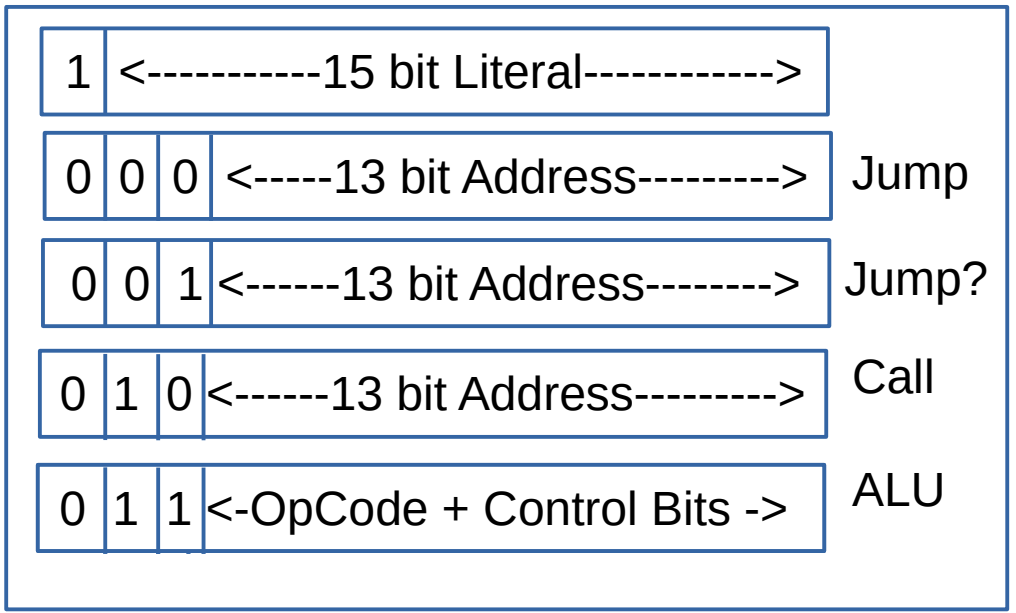
Memory Required

It is hard to compare soft core CPUs which are all very different. Best to compare the same application running on both a register and a stack machine.

Register Machine Version	Stack Machine Version
J1 Video application on 32 bit and 32 register Microblaze in C 16380 Bytes	J1 Video application on J1 in Forth. 6349 Bytes

J1 Vs RISC-V Memory

J1



RISC-V

3 * 5 bits for two operands and a results register and 7->17 bits OpCode = 22->32 bits

Fun7	Reg1	Reg2	Fun3	Result	OpCode

[Second Generation Stack Computer Architecture]

Stack Vs Register Machine Memory

Stack Machines

6-8 Bits for a Stack Machine Instruction. Eg: MicroCore UXN

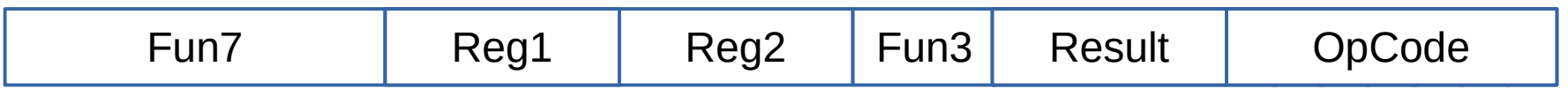
L = Literal

3 OpCodes in 16 bits. Eg EP16, b16

5 opCodes in 32 bits. Eg EP32

RISC-V

3 * 5 bits for two operands and a results register and 7->17 bits OpCode = 22->32 bits Risc-V



Second Generation Stack Computer Architecture

Forth BNF Parser

Program	Implementation Languages	Output	Source Lines	All Lines	Remark
bnfparse	Forth	-	14	16	
DCG	Prolog	Prolog	68	226	
mop	Perl	-	156	291	only Rule.pm (not Lex.pm)
Gray	Forth	bin. Forth	473	754	
kwParsing	Python	bin. Python	1691	2883	
Coco/R	Modula-2, Coco/R	Modula-2	4005	5106	
mlyacc	ML, mlyacc	ML	4395	6352	
rdp	C, rdp	C	4947	6519	
bison	C	C	7806	11258	
ell	Modula-2, Cocktail tools	Modula-2, C	8712	11384	
ANTLR	C, ANTLR	C	18577	23318	

If you want an infix Interpreter the Forth BNF parser is only 16 Lines of code.

Faster Stack Instructions

Stack based languages such require fewer instructions on stack based computers.

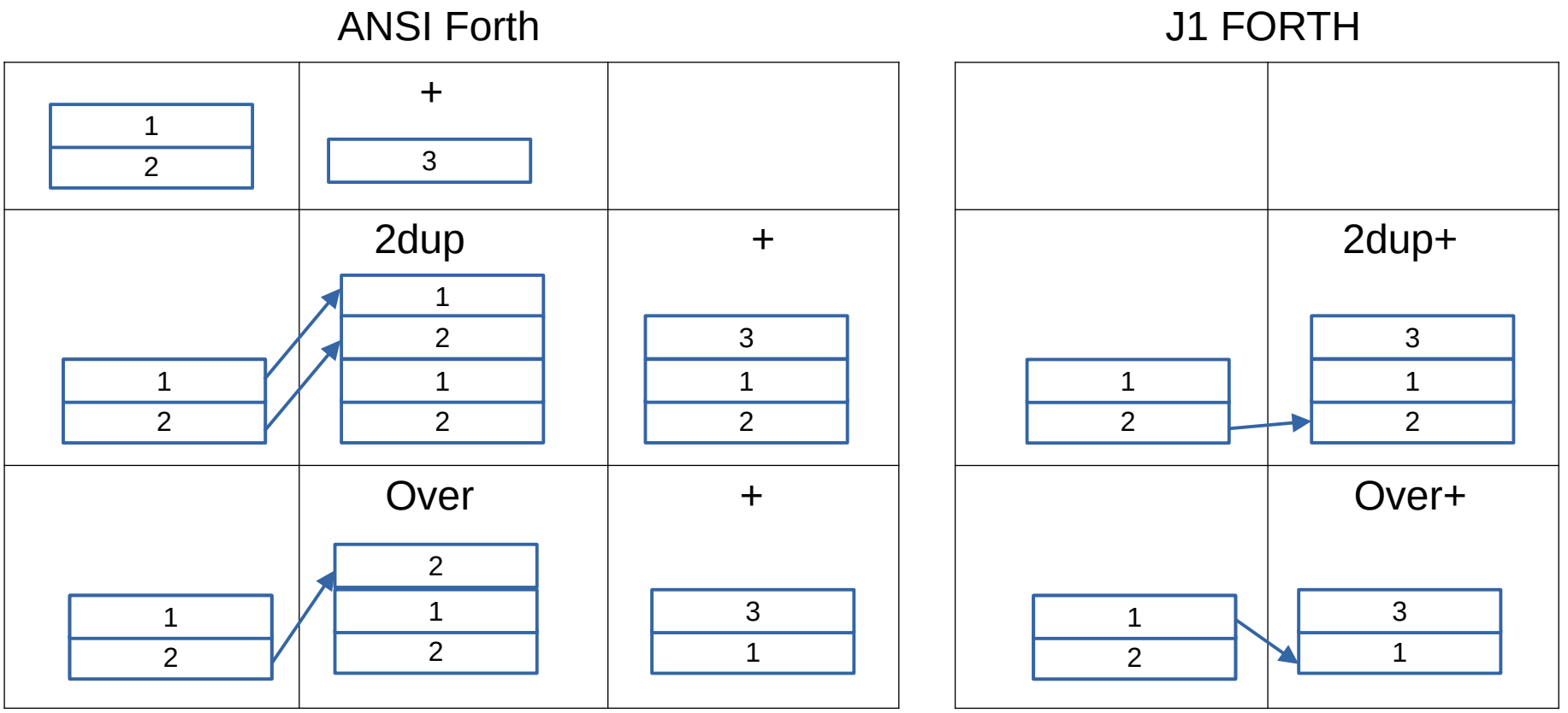
Operation	Stack effect	Forth CPU	Arm C

+	(x1 x2 -- sum)	+
		1 clock Cycle
			LDM pt2nd!, {r0}
			ADD pstop, r0, pstop
			2 instructions, 3 cycles

Swap	(x1 x2 – x2 x1)	Swap
		1 clock cycle
			LDR r0, [PT2ND]
			STR PSTOP, [PT2ND]
			MOV PSTOP, r0
			3 instructions, 5 clock cycles

Rotate3	(x1 x2 x3 –
	X3 X1 X2)
		Rot3
		1 clock cycle
			LDM pt2nd!, {r0, r1}
			STMDB pt2nd1 {r1, PSTOP}
			MOV PSTOP, r0
			3 instructions, 7 clock cycles

J1 Elided Words Vs ANSI Forth



Stack Machines

Stack Machine Speedup

VLIW J1 Instruction	Compatible instructions

Literal
Call
Jump (not conditional)
Stack Shuffle
Allocate Memory for Locals
Copy TOS to Locals Memory
Add Exception Handler
Single Operand + Dual Operand Instruction

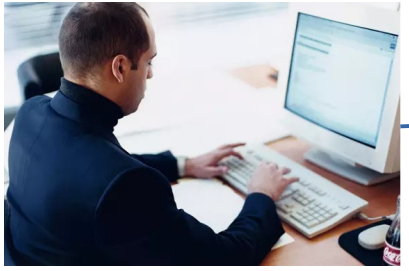
RISC-V

3 * 5 bits for two operands and a results register and 7->17 bits OpCode = 22->32 bit

Fun7	Reg1	Reg2	Fun3	Result	OpCode

Second Generation Stack Computer Architecture

Forth Co-Processors for Circuit Python



Questions

On an FPGA, a stack machine is simpler, smaller, faster, requires less memory and less power than a 32 bit 32 register register machine.

Christopher Lozinski

lozinski@PythonLinks.info

@PythonLinks@Mastodon.Social

Forth Discord Server

Pico-Ice Discord Server

Hana-1 Discord Channel